**Job Role Profile**

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|  | **Job Title:** | **Digital Design Engineer** | | |
|  | **Department:** | **Digital CDT or PDT or MDT, IoT Wi-Fi BU** | | |
|  | **Direct Supervisor:** | **Digital CDT or PDT or MDT Lead** | **Cost Centre:** | N/A |
|  | **Location:** | **Pangyo Office** | **Job Number/**  **Job Code:** | N/A |
|  | **Country:** | **Korea** | **Position Number:** | N/A |
| **1** | **Job Purpose:** | | | |
|  | * ASIC RTL design engineer * Good knowledge in design techniques and low power logic design * Good knowledge in architectures of CPU subsystem, especially ARM CPUs and AMBA subsystem, digital interfaces, and various digital components. | | | |
| **2** | **Dimensions:**   * No statistical or financial data relevant to the role | | | |
| **3** | **Principal Accountabilities**:   * RTL design and simulation verification of * CPU subsystem, especially using ARM CPU and AMBA subsystem architecture * Various digital interfaces such as I2C, SPI, UART, PWM, SDIO, eMMC, GPIO, etc * Various digital components such as FIFO, DMA, timers, memory controllers, cache controller, etc * FPGA design and verification (Xilinx or Intel) * DFT (Design For Testability) * ASIC top * Digital front-end jobs interfacing with layout engineers * Design and verification of digital modem design in terms of algorithm and RTL * Design and verification of security and cryptographic components in terms of algorithm and RTL * Collaboration with various kinds of people such as system architects, software engineers, verification engineers, RF/analog design engineers, etc * Documentations on everything one did. | | | |
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| **4** | **Key Performance Measures:**   * Achievement for the target goals * Problem solving capabilities * Design quality and documents, including functionality and timing * Commitment to the job | | | |
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| **5** | **Knowledge, Skills and Experience:** | | | |
|  | *Essential*   * Majoring in or experiencing * HDL language such as Verilog, System Verilog, VHDL, etc * EDA tools such as Cadence’s Virtuoso, Xcelium/Incisive/Simvision, Synopsys’ Design Compiler, PrimeTime, Test Compiler, Synplify, etc * RTL design including creating good test benches * design of some of CPU subsystems, especially using ARM CPUs and AMBA components * design of some of digital interfaces such as I2C, SPI, UART, PWM, SDIO, eMMC, GPIO, etc * design of some of digital components such as FIFO, DMA, timers, memory controllers, cache controller, etc * some of FPGA design (Xilinx or Intel) * Having good skill in UNIX, C/C++, and scripting languages like Tcl * Having good communication skill in collaborating with other people * Taking aggressive approach to meet the own development plan   *Desirable*   * Understand the overall application of the chips and developing improved design * Majoring in or experiencing * digital front-end * SoC tape-out * design of wide range of CPU subsystems, especially using ARM CPUs and AMBA components * design of wide range of digital interfaces such as I2C, SPI, UART, PWM, SDIO, eMMC, GPIO, etc * design of wide range of digital components such as FIFO, DMA, timers, memory controllers, cache controller, etc * extensive FPGA design (Xilinx or Intel) * Majoring in or experiencing digital signal processing * Majoring in or experiencing digital modem design in terms of algorithm and RTL design * Majoring in or experiencing security and cryptography in terms of theory and RTL design * Having good skill in Matlab or System C | | | |
| **6** | **Qualifications***:*   * MS or PHD in Electrical/Electronics Engineering | | | |
| **7** | **Key Relationships:**   * Design engineers within the same team and other RTL teams (Not all Korean) * Work closely with software teams (Not all Korean) * System Architect (Not Korean) * Team leader, group leader, and project leader | | | |
| **8** | **Organisation Chart:**  Reporting to: Digital CDT or PDT or MDT lead | | | |

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Employee name (in block letters)

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Employee Signature Date